C&C

OIPE IAP67 NOV 09 2005 PATENT & TRADEMARK OFFICE

DOCKET NO: S1022.80545US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Peter Ballam		
Serial No.:	09/692,422	Patent No.	6,959,271 B1
Filed:	October 19, 2000	Issued	October 25, 2005
For:	A METHOD OF IDENTIFYING AN ACCURATE MODEL		

Examiner:	Albert William Paladini		
Art Unit:	2125	Confirmation No:	6731

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate NOV 15 2005 of Correction

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: 04/23/04 Am; Relevant Pages Appl. as Filed, Title Page, Issue Fee Transmittal and Col 1, 4, 5-7, 9-11 and 15-20 of U.S. Patent No. 6,959,271
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 7nd day of November, 2005.

Gail Driscoll

Attorney Docket No.: S1022.80545US00
XNDD

Respectfully submitted,

Peter Ballam, Applicant

By: James Morris

James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

NOV 17 2005

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,959,271 B1
DATED : October 25, 2005
INVENTOR(S) : Peter Ballam

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item (74) should read:
(74) Attorney, Agent, or Firm –Lisa K. Jorgenson; James H. Morris; Wolf, Greenfield & Sacks, P.C.

Col. 1, line 50 should read:
behaviour of circuitry described using a hardware descrip-
line 60 should read:
as VHDL.

Col. 4, line 24 should read:
particular 'X' on an output can indicate that an error has

Col. 5, line 21 should read:
4. .ends

Col. 6, line 11 should read:
in one of the many supported simulators. Additional param-
line 13 should read:
These are then used to alter the behaviour of the tool and the

Col. 7, line 12 should read:
midband voltage using a weaker strength drive than
lines 23 and 24 should read:
carried out using the expanded logic package and the results are verified against the expected reference results from the VHDL
line 27 should read:
find potential bad transitions.

Col. 9, line 46 should read:
In the following, Rl can have a resistance of 100 Ohms, R2

Col. 10, line 1 should read:
have an approximate value of 100 k Ohms. The circuit 308 is

Col. 11, line 24 should read:
voltages. The stimulus for these are made by generating
line 24 should read:
/name/A:I STD_logic

Col. 15, line 22 should read:
0ns 0 0

MAILING ADDRESS OF SENDER

PATENT NO. 6,959,271

James H. Morris
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
~~~ton, Massachusetts 02210

NOV 17 2005
~~~

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,959,271 B1
DATED : October 25, 2005
INVENTOR(S) : Peter Ballam

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 16, line 14 should read:
original database. In steps S9, S10 and S11, the Xs are

Col. 17, line 39 should read:
and S14)

Col. 18, line 23 should read:
WP-W-PROGRESS, Percentage of vectors parsed=100% - completed

Col. 19, lines 34-35 should read:
results of the model with results from running an analog model of the circuit, identifying whether the digital model is

Col. 20, lines 23-24 should read:
said model;
means for re-running the model by applying said expanded set of signals to the model to obtain a
line 27 should read:
the second set of results and providing an output

MAILING ADDRESS OF SENDER

PATENT NO. 6,959,271

James H. Morris
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210

NOV 1 7 2005

DOCKET NO: S1022.80545US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Peter Ballam		
Serial No:	09/692,422	Patent No.	6,959,271 B1
Filed:	October 19, 2000	Issued	October 25, 2005
For:	A METHOD OF IDENTIFYING AN ACCURATE MODEL		

Examiner:	Albert William Paladini		
Art Unit:	2125	Confirmation No:	6731

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.323

Sir/Madam:

Patentee respectfully requests the correction of errors found in the above-captioned patent. Specifically, there are errors on the title page in item (74), in the specification and in claims 6 and 10 of issued U.S. Patent No. 6,959,271 B1.

In item (74), on the title page of U.S. Patent No. 6,959,271 the name of the firm that prosecuted the application has a misspelling. As it appears on the title page of U.S. Patent No. 6,959,271 the firm name reads: Wolf, Greenfield & **Saks**, P.C.

The correct name for the is Wolf, Greenfield & **Sacks**, P.C. as shown on the enclosed copy of the Issue Fee Transmittal.

Errors made in the specification are shown below: in column 1, the text as it appears in either the application as filed or in an amendment, in column 2 the corresponding text as it appears in issued U.S. Patent No. 6,959, 271 with the discrepancies indicated in bold text.

As Filed or Amended		U.S. Patent No. 6,959,271
As a solution to the task of describing circuits of such	1	As a solution to the task of describing circuits of such
large scale, digital simulators have been developed.	2	large scale, digital simulators have been developed.
Numerous digital simulators have been developed to	3	Numerous digital simulators have been developed to
model the behaviour of circuitry described using a	4	model the behaviour to of circuitry described using a
hardware description language (HDL). HDL is a	5	hardware description language (HDL). HDL is a
programming language which has been designed and	6	programming language which has been designed and
optimised for simulating and thereby describing	7	optimised for simulating and thereby describing
behaviour of digital circuitry. HDL allows electrical	8	behaviour of digital circuitry. HDL allows electrical
aspects of circuit behaviour be precisely described.	9	aspects of circuit behaviour to be precisely described.
However since only digital signals (which have one of	10	However since only digital signals (which have one of
two states) are simulated simulation time scales are	11	two states) are simulated simulation time scales are
much reduced. Additionally, only changes of logic	12	much reduced. Additionally, only changes of logic
level trigger an evaluation of the effect. A specific	13	level trigger an evaluation of the effect. A specific
example of HDL is the very high speed integrated	14	example of HDL is the very high speed integrated
circuit HDL known as VHDL.	15	circuit HDL known as VHDL.,
Page 2, lines 7-19		Column 1, lines 47-60

The word "to" in line 4 and the comma at the end of the paragraph, line 15, found in issued U.S. Patent No. 6,959,271 were not in the application as filed or introduced by any amendment made by the Examiner or inventor.

As Filed or Amended		U.S. Patent No. 6,959,271
'X': This also represents a strong unknown and can be	1	'X': This also represents a strong unknown and can be
anything from a strong low to a strong high signal. In	2	anything from a strong low to a strong high signal. In
particular 'X' on an output can indicate that an error	3	**articular** 'X' on an output can indicate that an error
has occurred as the signal has passed through the	4	has occurred as the signal has passed through the
model.	5	model.
Page 6, line 37-page 7, line 2		Column 4, lines 22-25

A typographical error in the word "articular" in line 3, found in issued U.S. Patent No. 6,959,271 should read "particular".

As Filed or Amended		U.S. Patent No. 6,959,271
4. .ends	1	4. ends
Page 8, last line		Column 5, line 21

The above line should read 4..ends.

As Filed or Amended		U.S. Patent No. 6,959,271
Embodiments of the present invention use WIF files. A WIF (waveform interface format) file is an ASCII based file which contains information needed to describe the model's interface (names of ports, directions of signals - input/output/bi-directional, and types of signals) and signal activity against time in a tabular format. In embodiments of the present invention, the IEEE 9 logic states discussed previously are used to indicate both driven and driving states. The pin direction is then used to determine what needs to be done to either drive the value or test for the existence of a value in one of the many supported simulators. **Additional** parameters can be specified using specially defined comments. These are then used to alter the **behaviour** of the tool and the simulations/interpretations performed by the tool.		Embodiments of the present invention use WIF files. A WIF (waveform interface format) file is an ASCII based file which contains information needed to describe the model's interface (names of ports, directions of signals - input/output/bi-directional, and types of signals) and signal activity against time in a tabular format. In embodiments of the present invention, the IEEE 9 logic states discussed previously are used to indicate both driven and driving states. The pin direction is then used to determine what needs to be done to either drive the value or test for the existence of a value in one of the many supported simulators. **Addistional** parameters can be specified using specially defined comments. These are then used to alter the **behavious** of the tool and the simulations/interpretations performed by the tool.
Page 10, lines 12-25		Column 6, lines 1-14

The above appear to be typographical errors found in U.S. Patent No. 6,959,271 wherein the words "additional" and "behaviour" in lines 13 and 15 respectively have been misspelled.

As Filed or Amended		U.S. Patent No. 6,959,271
All this data is then used to write an ELDO test bench that connects to the cell's inputs via a digital to analog converter (DAC) and which can drive the pin to a high or low voltage with different drive strengths. The test bench can also set up a potential divider to provide midband voltages. The actual type of DAC is determined for each pin depending upon what logic states it needs to produce for the simulation. For normal output pins a potential divider is connected to effectively try to force the output pin to a weak unknown. For pins with varying strengths of output another type of DAC is connected that always tries to drive the pin to a midband voltage using a weaker strength drive than should be present on the output. For an output at high impedance a very weak drive is used to drive the pin low then high to try to prove the pin is floating. All the information to do this is held in the program's working memory.		All this data is then used to write an ELDO test bench that connects to the cell's inputs via a digital to analog converter (DAC) and which can drive the pin to a high or low voltage with different drive strengths. The test bench can also set up a potential divider to provide midband voltages. The actual type of DAC is determined for each pin depending upon what logic states it needs to produce for the simulation. For normal output pins a potential divider is connected to effectively try to force the output pin to a weak unknown. For pins with varying strengths of output another type of DAC is connected that always tries to drive the pin to a midband **in** voltage using a weaker strength drive than should be present on the output. For an output at high impedance a very weak drive is used to drive the pin low then high to try to prove the pin is floating. All the information to do this is held in the program's working memory.
Page 12, lines 5-20		Column 7, lines 1-16

The word "in" in line 13, found in issued U.S. Patent No. 6,959,271 was not in the application as filed or introduced by any amendment made by the Examiner or inventor.

As Filed or Amended		U.S. Patent No. 6,959,271
The third stage takes place after the ELDO simulation	1	The third stage takes place after the ELDO simulation
is carried out using the expanded **logic** package and	2	is carried out using the expanded **logiic** package and
the results are verified against the expected reference	3	the results are verified against the expected reference
results from the VHDL simulation. Not only can the	4	from the VHDL simulation. Not only can the tool
tool check that the outputs match but further	5	check that the outputs match but further verifications
verifications can be made to the results to find	6	can be made to the results to find potential bad
potential bad **transitions**.	7	**transistions**.
Page 12, April 23, 2004 amendment		Column 7, lines 22-27

The above appear to be typographical errors found in U.S. Patent No. 6,959,271 wherein the words "logic" and "transitions" in lines 2 and 7, respectively, have been misspelled. Additionally, the word "results" found in the application as filed on page 12, line 30 has been omitted (line 4 above).

As Filed or Amended		U.S. Patent No. 6,959,271
In the following, Rl can have a resistance of **100**	1	In the following, Rl can have a resistance of **1000**
Ohms, R2 a resistance 100 K Ohms, R3 a resistance	2	**hms**, R2 a resistance 100 K Ohms, R3 a resistance of
of 250 K Ohms and R4 a resistance of 1 MegaOhm.	3	250 K Ohms and R4 a resistance of 1 MegaOhm.
These values are by way of example only.	4	These values are by way of example only.
	5	
Page 17, lines 9-12		Column 9, lines 46-49

The resistance "1000hms" in line 1 above and as shown in issued U.S. Patent No. 6,959,271 should read "100 Ohms".

As Filed or Amended		U.S. Patent No. 6,959,271
The following are used by the third algorithm. Signal	1	The following are used by the third algorithm. Signal
generating circuits **308** and **309** each include a voltage	2	generating circuits **308** and **309** each include a voltage
control switch connected to a resistor R2. These	3	control switch connected to a resistor R2. These
resistors have an approximate value of **100 kOhms.**	4	resistors have an approximate value of **100 kohms.**
The circuit **308** is connected to the ground line whilst	5	The circuit **308** is connected to the ground line whilst
circuit **309** is connected to the high voltage supply	6	circuit **309** is connected to the high voltage supply
line VDD. Each voltage controlled switch is operable	7	line VDD. Each voltage controlled switch is operable
in response to control signals input on control input	8	in response to control signals input on control input
terminals **310** and **311** respectively. The inputs on	9	terminals **310** and **311** respectively. The inputs on
these terminals will be a series of 0's and 1's produced	10	these terminals will be a series of 0's and 1's produced

by the WIF2TB tool to control the operation of the	11	by the WIF2TB tool to control the operation of the
circuits **308** and **309**. The outputs of these two circuits	12	circuits **308** and **309**. The outputs of these two circuits
are connected to node **314** which is connected to an	13	are connected to node **314** which is connected to an
input of the hardware cell.	14	input of the hardware cell.
Page 17, line 31 through page 18, line 4		Columns 9, line 65 through column 10, line 10

The value “100 kohms” in line 4 above and as shown in issued U.S. Patent No. 6,959,271 should read “100 kOhms”.

As Filed or Amended		U.S. Patent No. 6,959,271
Any signals left to generate are a mix of drive	1	Any signals left to generate are a mix of drive
strengths and logic levels. These cases may also have	2	strengths and logic levels. These cases may also have
midband voltages. The **stimulus** for these are made	3	midband voltages. The **stimuls** for these are made by
by generating control sequences from pattern	4	generating control sequences from pattern generating
generating voltage sources that switch on and off the	5	voltage sources that switch on and off the voltage
voltage controlled switches. Each switch connects to	6	controlled switches. Each switch connects to the
the required supply by the required resistor. The	7	required supply by the required resistor. The pattern
pattern generating control supplies are named using	8	generating control supplies are named using numbers
numbers to identify the required effect. These are	9	to identify the required effect. These are index
index numbers. When a 1 is output the corresponding	10	numbers. When a 1 is output the corresponding
voltage and drive strength determined by the resistor	11	voltage and drive strength determined by the resistor
used is output. When the control sequence signal is	12	used is output. When the control sequence signal is
low on a voltage controlled switch the element is	13	low on a voltage controlled switch the element is
tristated from the pin. The following table defines	14	tristated from the pin. The following table defines
what the index number of each control voltage drives:	15	what the index number of each control voltage drives:
Page 20, lines 4-16		Column 11, lines 22-35

The word “stimulus” on line 3 above appears to be a typographical error.

As Filed or Amended		U.S. Patent No. 6,959,271
/name/A:I STD_**logic**	1	/name/A:I STD_**log2 c**
Page 21, line 7		Column 11, line 55

The word “log2 c” in line 1 above and as shown in issued U.S. Patent No. 6,959,271 should read “logic”.

As Filed or Amended		U.S. Patent No. 6,959,271
Ons: 0 0	1	Ons: 0 0
Page 27, line 30		Column 15, line 22

The first result “Ons: 0 0” in line 1 above and as shown in issued U.S. Patent No. 6,959,271 should read “0ns: 0 0”.

As Filed or Amended		U.S. Patent No. 6,959,271
In step S7, a second WIF file for the outputs is read into memory. In step **S8**, the output patterns are copied into the original database. In steps **S9**, **S10** and **S11**, the Xs are expanded. 'X's are expanded. In step S9, level sensitive 'X's are expanded. In step **S10** edge sensitive X's are expanded. In step **S11**, double edged 'X's are expanded	1 2 3 4 5 6 7	In step S7, a second WIF file for the outputs is read into memory. In step **S8**, the output patterns are copied into the original database. In steps **S9**, **S10** and **S81**, the Xs are expanded. 'X's are expanded. In step S9, level sensitive 'X's are expanded. In step **S10** edge sensitive X's are expanded. In step **S11**, double edged 'X's are expanded
Page 29, lines 19-24		Column 16, lines 12-17

The listing of the steps “**S9**, **S10** and **S81**” in lines 3 and 4 above and as shown in issued U.S. Patent No. 6,959,271 should read “**S9**, **S10** and **S11**”.

As Filed or Amended		U.S. Patent No. 6,959,271
SECTION 11—the second HDL simulation (steps S13 and S14)	1 2	SECTION 11—the second HDL simulation (steps S13 and **514**)
Page 32, line 3		Column 17, lines 38-39

The listing of the steps “**S13** and **514**” in line 2 above and as shown in issued U.S. Patent No. 6,959,271 should read “**S13** and **S14**”.

As Filed or Amended		U.S. Patent No. 6,959,271
WP-W-PROGRESS, Percentage of vectors parsed=100% - completed	1 2	WP-W-PROGRESS, Percentage of vectors parsed=100k - completed
Page 33, line 18		Column 18, line 23

The percentage of vectors parsed “100k” in line 2 above and as shown in issued U.S. Patent No. 6,959,271 should read “100%”.

Errors to the claims are identified below.

Claim 6 as it appeared on page 7 of the Amendment filed January 23, 2004 is reproduced below.

> 6. A method according to claim 1, further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with results from running an analog model of the circuit, **identifying** whether the digital model is an accurate model and only comparing the digital model results with the analog model results if the digital model is determined to be accurate. (Emphasis added)

Claim 6, as it appears in column 19, line 32 through column 20, line 2 is reproduced below.

> 6. A method according to claim 1, further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with results from **of** running an analog model of the circuit, **identfying** whether the digital model is an accurate model and only comparing the digital model results with the analog model results if the digital model is determined to be accurate. (Emphasis added)

No amendment was made by the Examiner or Patentee to insert the word "of" between "from" and "running" on line 35 of this claim. Additionally, there is a misspelling of the word "identifying" on line 36 of the issued patent that is not found in the January 23, 2004 amendment of this claim.

Claim 10 as it appeared on page 8 of the Amendment filed January 23, 2004 is reproduced below.

> 10. A system for identifying an inaccurate model of a hardware circuit comprising:
>
> means for running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level;
>
> means for replacing the at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;
>
> means for re-running **the** model by applying said expanded set of **signals** to the model to obtain a second set of results; and
>
> means for comparing the first set of expected results with the second set of results and providing **an** output signal indicating that the model is inaccurate if

the first set of expected results and the second set of results contradict. (Emphasis added)

Claim 10 as it appears in column 20, lines 15-39 is reproduced below.

10. A system for identifying an inaccurate model of a hardware circuit comprising:

means for running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level;

means for replacing the at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model; ¶means for re-running model by applying said expanded set of **signal** to the model to obtain a second set of results; and

means for comparing the first set of expected results with the second set of results and providing **and** output signal indicating that the model is inaccurate if the first set of expected results and the second set of results contradict. (Emphasis added)

No amendment was made by the Examiner or Patentee to delete the paragraph break or to delete the word "the" in column 20, line 23 or to change "signals" to "signal" in column 20, line 24, or to change "an" to "and" in column 20, line 27.

In support of the above, Patentee encloses a highlighted copies of: the April 23, 2004 amendment; relevant pages of the application as filed, title page and columns 1, 4, 5-7, 9-11 and 15-20 of U.S. Patent No. 6,959,271. Also enclosed is a Certificate of Correction form, PTO Form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Since neither of the above amendments were made by either Patentee or the Examiner. Patentee respectfully submits that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 7nd day of November, 2005.

Attorney Docket No.: S1022.80545US00
XNDD

Respectfully submitted,

Peter Ballam, Applicant

By:

James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

DOCKET NO: S1022.80545US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Peter Ballam		
Serial No:	09/692,422	Patent No.	6,959,271
Filed:	October 19, 2000	Issued	October 25, 2005
For:	A METHOD OF IDENTIFYING AN ACCURATE MODEL		
Examiner:	Albert William Paladini		
Art Unit:	2125	Confirmation No:	6731

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.323

Sir/Madam:

Patentee respectfully requests the correction of errors found in the above-captioned patent. Specifically, there are errors on the title page in item (74), in the specification and in claims 6 and 10 of issued U.S. Patent No. 6,959,271 B1.

In item (74), on the title page of U.S. Patent No. 6,959,271 the name of the firm that prosecuted the application has a misspelling. As it appears on the title page of U.S. Patent No. 6,959,271 the firm name reads: Wolf, Greenfield & **Saks**, P.C.

The correct name for the is Wolf, Greenfield & **Sacks**, P.C. as shown on the enclosed copy of the Issue Fee Transmittal.

Errors made in the specification are shown below: in column 1, the text as it appears in either the application as filed or in an amendment, in column 2 the corresponding text as it appears in issued U.S. Patent No. 6,959, 271 with the discrepancies indicated in bold text.

As Filed or Amended		U.S. Patent No. 6,959,271
As a solution to the task of describing circuits of such	1	As a solution to the task of describing circuits of such
large scale, digital simulators have been developed.	2	large scale, digital simulators have been developed.
Numerous digital simulators have been developed to	3	Numerous digital simulators have been developed to
model the behaviour of circuitry described using a	4	model the behaviour to of circuitry described using a
hardware description language (HDL). HDL is a	5	hardware description language (HDL). HDL is a
programming language which has been designed and	6	programming language which has been designed and
optimised for simulating and thereby describing	7	optimised for simulating and thereby describing
behaviour of digital circuitry. HDL allows electrical	8	behaviour of digital circuitry. HDL allows electrical
aspects of circuit behaviour be precisely described.	9	aspects of circuit behaviour to be precisely described.
However since only digital signals (which have one of	10	However since only digital signals (which have one of
two states) are simulated simulation time scales are	11	two states) are simulated simulation time scales are
much reduced. Additionally, only changes of logic	12	much reduced. Additionally, only changes of logic
level trigger an evaluation of the effect. A specific	13	level trigger an evaluation of the effect. A specific
example of HDL is the very high speed integrated	14	example of HDL is the very high speed integrated
circuit HDL known as VHDL.	15	circuit HDL known as VHDL.,
Page 2, lines 7-19		Column 1, lines 47-60

The word "to" in line 4 and the comma at the end of the paragraph, line 15, found in issued U.S. Patent No. 6,959,271 were not in the application as filed or introduced by any amendment made by the Examiner or inventor.

As Filed or Amended		U.S. Patent No. 6,959,271
'X': This also represents a strong unknown and can be	1	'X': This also represents a strong unknown and can be
anything from a strong low to a strong high signal. In	2	anything from a strong low to a strong high signal. In
particular 'X' on an output can indicate that an error	3	**articular** 'X' on an output can indicate that an error
has occurred as the signal has passed through the	4	has occurred as the signal has passed through the
model.	5	model.
Page 6, line 37-page 7, line 2		Column 4, lines 22-25

A typographical error in the word "articular" in line 3, found in issued U.S. Patent No. 6,959,271 should read "particular".

As Filed or Amended		U.S. Patent No. 6,959,271
4. .ends	1	4. ends
Page 8, last line		Column 5, line 21

The above line should read 4..ends.

As Filed or Amended		U.S. Patent No. 6,959,271
Embodiments of the present invention use WIF files.	1	Embodiments of the present invention use WIF files.
A WIF (waveform interface format) file is an ASCII	2	A WIF (waveform interface format) file is an ASCII
based file which contains information needed to	3	based file which contains information needed to
describe the model's interface (names of ports,	4	describe the model's interface (names of ports,
directions of signals - input/output/bi-directional, and	5	directions of signals - input/output/bi-directional, and
types of signals) and signal activity against time in a	6	types of signals) and signal activity against time in a
tabular format. In embodiments of the present	7	tabular format. In embodiments of the present
invention, the IEEE 9 logic states discussed	8	invention, the IEEE 9 logic states discussed
previously are used to indicate both driven and	9	previously are used to indicate both driven and
driving states. The pin direction is then used to	10	driving states. The pin direction is then used to
determine what needs to be done to either drive the	11	determine what needs to be done to either drive the
value or test for the existence of a value in one of the	12	value or test for the existence of a value in one of the
many supported simulators. **Additional** parameters	13	many supported simulators. **Addistional** parameters
can be specified using specially defined comments.	14	can be specified using specially defined comments.
These are then used to alter the **behaviour** of the tool	15	These are then used to alter the **behavious** of the tool
and the simulations/interpretations performed by the	16	and the simulations/interpretations performed by the
tool.	17	tool.
Page 10, lines 12-25		Column 6, lines 1-14

The above appear to be typographical errors found in U.S. Patent No. 6,959,271 wherein the words "additional" and "behaviour" in lines 13 and 15 respectively have been misspelled.

As Filed or Amended		U.S. Patent No. 6,959,271
All this data is then used to write an ELDO test bench	1	All this data is then used to write an ELDO test bench
that connects to the cell's inputs via a digital to analog	2	that connects to the cell's inputs via a digital to analog
converter (DAC) and which can drive the pin to a	3	converter (DAC) and which can drive the pin to a
high or low voltage with different drive strengths. The	4	high or low voltage with different drive strengths. The
test bench can also set up a potential divider to	5	test bench can also set up a potential divider to
provide midband voltages. The actual type of DAC is	6	provide midband voltages. The actual type of DAC is
determined for each pin depending upon what logic	7	determined for each pin depending upon what logic
states it needs to produce for the simulation. For	8	states it needs to produce for the simulation. For
normal output pins a potential divider is connected to	9	normal output pins a potential divider is connected to
effectively try to force the output pin to a weak	10	effectively try to force the output pin to a weak
unknown. For pins with varying strengths of output	11	unknown. For pins with varying strengths of output
another type of DAC is connected that always tries to	12	another type of DAC is connected that always tries to
drive the pin to a midband voltage using a weaker	13	drive the pin to a midband **in** voltage using a weaker
strength drive than should be present on the output.	14	strength drive than should be present on the output.
For an output at high impedance a very weak drive is	15	For an output at high impedance a very weak drive is
used to drive the pin low then high to try to prove the	16	used to drive the pin low then high to try to prove the
pin is floating. All the information to do this is held in	17	pin is floating. All the information to do this is held in
the program's working memory.	18	the program's working memory.
Page 12, lines 5-20		Column 7, lines 1-16

The word "in" in line 13, found in issued U.S. Patent No. 6,959,271 was not in the application as filed or introduced by any amendment made by the Examiner or inventor.

As Filed or Amended		U.S. Patent No. 6,959,271
The third stage takes place after the ELDO simulation	1	The third stage takes place after the ELDO simulation
is carried out using the expanded **logic** package and	2	is carried out using the expanded **logiic** package and
the results are verified against the expected reference	3	the results are verified against the expected reference
results from the VHDL simulation. Not only can the	4	from the VHDL simulation. Not only can the tool
tool check that the outputs match but further	5	check that the outputs match but further verifications
verifications can be made to the results to find	6	can be made to the results to find potential bad
potential bad **transitions**.	7	**transistions**.
Page 12, April 23, 2004 amendment		Column 7, lines 22-27

The above appear to be typographical errors found in U.S. Patent No. 6,959,271 wherein the words "logic" and "transitions" in lines 2 and 7, respectively, have been misspelled. Additionally, the word "results" found in the application as filed on page 12, line 30 has been omitted (line 4 above).

As Filed or Amended		U.S. Patent No. 6,959,271
In the following, Rl can have a resistance of **100**	1	In the following, Rl can have a resistance of **1000**
Ohms, R2 a resistance 100 K Ohms, R3 a resistance	2	**hms**, R2 a resistance 100 K Ohms, R3 a resistance of
of 250 K Ohms and R4 a resistance of 1 MegaOhm.	3	250 K Ohms and R4 a resistance of 1 MegaOhm.
These values are by way of example only.	4	These values are by way of example only.
	5	
Page 17, lines 9-12		Column 9, lines 46-49

The resistance "1000hms" in line 1 above and as shown in issued U.S. Patent No. 6,959,271 should read "100 Ohms".

As Filed or Amended		U.S. Patent No. 6,959,271
The following are used by the third algorithm. Signal	1	The following are used by the third algorithm. Signal
generating circuits **308** and **309** each include a voltage	2	generating circuits **308** and **309** each include a voltage
control switch connected to a resistor **R2**. These	3	control switch connected to a resistor **R2**. These
resistors have an approximate value of **100 kOhms**.	4	resistors have an approximate value of **100 kohms**.
The circuit **308** is connected to the ground line whilst	5	The circuit **308** is connected to the ground line whilst
circuit **309** is connected to the high voltage supply	6	circuit **309** is connected to the high voltage supply
line VDD. Each voltage controlled switch is operable	7	line VDD. Each voltage controlled switch is operable
in response to control signals input on control input	8	in response to control signals input on control input
terminals **310** and **311** respectively. The inputs on	9	terminals **310** and **311** respectively. The inputs on
these terminals will be a series of 0's and 1's produced	10	these terminals will be a series of 0's and 1's produced

by the WIF2TB tool to control the operation of the circuits **308** and **309**. The outputs of these two circuits are connected to node **314** which is connected to an input of the hardware cell.	11 12 13 14	by the WIF2TB tool to control the operation of the circuits **308** and **309**. The outputs of these two circuits are connected to node **314** which is connected to an input of the hardware cell.
Page 17, line 31 through page 18, line 4		Columns 9, line 65 through column 10, line 10

The value "100 kohms" in line 4 above and as shown in issued U.S. Patent No. 6,959,271 should read "100 kOhms".

As Filed or Amended		U.S. Patent No. 6,959,271
Any signals left to generate are a mix of drive strengths and logic levels. These cases may also have midband voltages. The **stimulus** for these are made by generating control sequences from pattern generating voltage sources that switch on and off the voltage controlled switches. Each switch connects to the required supply by the required resistor. The pattern generating control supplies are named using numbers to identify the required effect. These are index numbers. When a 1 is output the corresponding voltage and drive strength determined by the resistor used is output. When the control sequence signal is low on a voltage controlled switch the element is tristated from the pin. The following table defines what the index number of each control voltage drives:	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	Any signals left to generate are a mix of drive strengths and logic levels. These cases may also have midband voltages. The **stimuls** for these are made by generating control sequences from pattern generating voltage sources that switch on and off the voltage controlled switches. Each switch connects to the required supply by the required resistor. The pattern generating control supplies are named using numbers to identify the required effect. These are index numbers. When a 1 is output the corresponding voltage and drive strength determined by the resistor used is output. When the control sequence signal is low on a voltage controlled switch the element is tristated from the pin. The following table defines what the index number of each control voltage drives:
Page 20, lines 4-16		Column 11, lines 22-35

The word "stimulus" on line 3 above appears to be a typographical error.

As Filed or Amended		U.S. Patent No. 6,959,271
/name/A:I STD_**logic**	1	/name/A:I STD_**log2 c**
Page 21, line 7		Column 11, line 55

The word "log2 c" in line 1 above and as shown in issued U.S. Patent No. 6,959,271 should read "logic".

As Filed or Amended		U.S. Patent No. 6,959,271
0ns: 0 0	1	Ons: 0 0
Page 27, line 30		Column 15, line 22

The first result "Ons: 0 0" in line 1 above and as shown in issued U.S. Patent No. 6,959,271 should read "0ns: 0 0".

As Filed or Amended		U.S. Patent No. 6,959,271
In step S7, a second WIF file for the outputs is read into memory. In step S8, the output patterns are copied into the original database. In steps S9, S10 and S11, the Xs are expanded. 'X's are expanded. In step S9, level sensitive 'X's are expanded. In step S10 edge sensitive X's are expanded. In step S11, double edged 'X's are expanded	1 2 3 4 5 6 7	In step S7, a second WIF file for the outputs is read into memory. In step S8, the output patterns are copied into the original database. In steps S9, S10 and S81, the Xs are expanded. 'X's are expanded. In step S9, level sensitive 'X's are expanded. In step S10 edge sensitive X's are expanded. In step S11, double edged 'X's are expanded
Page 29, lines 19-24		Column 16, lines 12-17

The listing of the steps "S9, S10 and S81" in lines 3 and 4 above and as shown in issued U.S. Patent No. 6,959,271 should read "S9, S10 and S11".

As Filed or Amended		U.S. Patent No. 6,959,271
SECTION 11—the second HDL simulation (steps S13 and S14)	1 2	SECTION 11—the second HDL simulation (steps S13 and 514)
Page 32, line 3		Column 17, lines 38-39

The listing of the steps "S13 and 514" in line 2 above and as shown in issued U.S. Patent No. 6,959,271 should read "S13 and S14".

As Filed or Amended		U.S. Patent No. 6,959,271
WP-W-PROGRESS, Percentage of vectors parsed=100% - completed	1 2	WP-W-PROGRESS, Percentage of vectors parsed=100k - completed
Page 33, line 18		Column 18, line 23

The percentage of vectors parsed "100k" in line 2 above and as shown in issued U.S. Patent No. 6,959,271 should read "100%".

Errors to the claims are identified below.

Claim 6 as it appeared on page 7 of the Amendment filed January 23, 2004 is reproduced below.

> 6. A method according to claim 1, further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with results from running an analog model of the circuit, **identifying** whether the digital model is an accurate model and only comparing the digital model results with the analog model results if the digital model is determined to be accurate. (Emphasis added)

Claim 6, as it appears in column 19, line 32 through column 20, line 2 is reproduced below.

> 6. A method according to claim 1, further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with results from **of** running an analog model of the circuit, **identfying** whether the digital model is an accurate model and only comparing the digital model results with the analog model results if the digital model is determined to be accurate. (Emphasis added)

No amendment was made by the Examiner or Patentee to insert the word "of" between "from" and "running" on line 35 of this claim. Additionally, there is a misspelling of the word "identifying" on line 36 of the issued patent that is not found in the January 23, 2004 amendment of this claim.

Claim 10 as it appeared on page 8 of the Amendment filed January 23, 2004 is reproduced below.

> 10. A system for identifying an inaccurate model of a hardware circuit comprising:
>
> means for running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level;
>
> means for replacing the at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;
>
> means for re-running **the** model by applying said expanded set of **signals** to the model to obtain a second set of results; and
>
> means for comparing the first set of expected results with the second set of results and providing **an** output signal indicating that the model is inaccurate if

the first set of expected results and the second set of results contradict. (Emphasis added)

Claim 10 as it appears in column 20, lines 15-39 is reproduced below.

> 10. A system for identifying an inaccurate model of a hardware circuit comprising:
>
> means for running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level;
>
> means for replacing the at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model; ¶means for re-running model by applying said expanded set of **signal** to the model to obtain a second set of results; and
>
> means for comparing the first set of expected results with the second set of results and providing **and** output signal indicating that the model is inaccurate if the first set of expected results and the second set of results contradict. (Emphasis added)

No amendment was made by the Examiner or Patentee to delete the paragraph break or to delete the word "the" in column 20, line 23 or to change "signals" to "signal" in column 20, line 24, or to change "an" to "and" in column 20, line 27.

In support of the above, Patentee encloses a highlighted copies of: the April 23, 2004 amendment; relevant pages of the application as filed, title page and columns 1, 4, 5-7, 9-11 and 15-20 of U.S. Patent No. 6,959,271. Also enclosed is a Certificate of Correction form, PTO Form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Since neither of the above amendments were made by either Patentee or the Examiner. Patentee respectfully submits that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 7th day of November, 2005.

Attorney Docket No.: S1022.80545US00
XNDD

Respectfully submitted,

Peter Ballam, Applicant

By:

James H. Morris, Reg. No.: 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
Tel. (617) 720-3500

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,959,271
DATED : October 25, 2005
INVENTOR(S) : Peter Ballam

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item (74) should read:
(74) Attorney, Agent, or Firm –Lisa K. Jorgenson; James H. Morris; Wolf, Greenfield & Sacks, P.C.

Col. 1, line 50 should read:
behaviour of circuitry described using a hardware descrip-
line 60 should read:
as VHDL.

Col. 4, line 24 should read:
particular 'X' on an output can indicate that an error has

Col. 5, line 21 should read:
4. .ends

Col. 6, line 11 should read:
in one of the many supported simulators. Additional param-
line 13 should read:
These are then used to alter the behaviour of the tool and the

Col. 7, line 12 should read:
midband voltage using a weaker strength drive than
lines 23 and 24 should read:
carried out using the expanded logic package and the results are verified against the expected reference results from the VHDL
line 27 should read:
find potential bad transitions.

Col. 9, line 46 should read:
In the following, Rl can have a resistance of 100 Ohms, R2

Col. 10, line 1 should read:
have an approximate value of 100 k Ohms. The circuit 308 is

Col. 11, line 24 should read:
voltages. The stimulus for these are made by generating
line 24 should read:
/name/A:I STD_logic

Col. 15, line 22 should read:
0ns 0 0

MAILING ADDRESS OF SENDER

PATENT NO. 6,959,271

James H. Morris
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,959,271
DATED : October 25, 2005
INVENTOR(S) : Peter Ballam

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 16, line 14 should read:
original database. In steps S9, S10 and S11, the Xs are

Col. 17, line 39 should read:
and S14)

Col. 18, line 23 should read:
WP-W-PROGRESS, Percentage of vectors parsed=100% - completed

Col. 19, lines 34-35 should read:
results of the model with results from running an analog model of the circuit, identifying whether the digital model is

Col. 20, lines 23-24 should read:
said model;
means for re-running the model by applying said expanded set of signals to the model to obtain a
line 27 should read:
the second set of results and providing an output

MAILING ADDRESS OF SENDER

PATENT NO. 6,959,271

James H. Morris
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210

DOCKET NO: S1022.80545US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Peter Ballam
Serial No:	09/692,422
Confirmation No:	6731
Filed:	October 19, 2000
For:	A METHOD OF IDENTIFYING AN ACCURATE MODEL
Examiner:	Albert William Paladini
Art Unit:	2125

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 23rd day of April, 2004.

Donna V. Reed
Signature

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed December 24, 2003 please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this amendment.

Amendments to the Abstract begin on page 5 of this amendment.

Amendments to the Claims are reflected in the listing of claims that begins on page 6 of this amendment.

Remarks begin on page 9 of this amendment.

<u>In the Specification</u>

Applicant presents replacement and amended paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

On page 1 before line 2 please insert the heading as follows:
<u>Field of the Invention</u>

On page 1, before line 6 please insert the heading as follows:
<u>Background of the Invention</u>

Please amend the paragraph beginning at page 3, line 10 as follows:
VHDL supports many abstract data types which are used to ~~described~~ <u>describe</u> different signal strengths or commonly used simulation conditions such as unknowns and high-impedance conditions. These non-standard data types have been adopted by the IEEE as standard 1164. Such data types are not applicable to analog simulators which require true analog signals rather than abstract data types.

On page 3, before line 17 please insert the heading as follows:
<u>Summary of the Invention</u>

Please amend the paragraph beginning at page 3, line 21 as follows:
According to a first aspect of the present invention there is provided a method of identifying an inaccurate model of a hardware circuit comprising the steps of simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type <u>level</u> ~~are~~ to provide a set of expected results; replacing the ~~or each~~ <u>at least one</u> abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model; resimulating the model with said expanded set; and comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

Please amend the paragraph beginning at page 4, line 18 as follows:

According to a second aspect of the present invention, there is provided a system for identifying an inaccurate model of a hardware circuit comprising means for simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type level to provide a set of expected results; means for replacing the ~~or each~~ at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model; means for resimulating the model with said expanded set; means for comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

On page 4, before line 31 please insert the heading as follows:

Description of the Drawings

Please amend the paragraph beginning at page 4, line 35 as follows:

Figure 2 illustrates an inverter logic gate as ~~modelled~~ modeled by an analog model;

On page 5, before line 7 please insert the heading as follows:

Detailed Description

Please amend the paragraph beginning at page 7, line 17 as follows:

'H' : This is exactly the same as an 'L' however in the opposite sense, that is to say it represents a weak high.

Please amend the paragraph beginning at page 10, line 12 as follows:

Embodiments of the present invention use WIF files. A WIF (waveform interface format) file is an ASCII based file which contains information needed to describe the model's interface (names of ports, directions of signals – input/output/bi-directional, and types of signals) and signal activity against time in a tabular format. In embodiments of the present invention, the IEEE 9 logic states discussed previously are used to indicate both driven and driving states. The pin

direction is then used to determine what needs to be done to either drive the value or test for the existence of a value in one of the many supported simulators. Additional parameters can be ~~spec5ified~~ specified using specially defined comments. These are then used to alter the behaviour of the tool and the simulations/interpretations performed by the tool.

Please amend the paragraph beginning at page 12, line 28 as follows:

The third stage takes place after the ELDO simulation is carried out using the expanded logic package and the results are verified against the expected reference results from the VHDL simulation. Not only can the tool check that the outputs match but further verifications can be made to the results to find potential bad transitions.

In the Abstract

Please amend the Abstract beginning at page 37, as follows:

A method is described for identifying an inaccurate model of a hardware circuit. The method includes the steps of simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type level to provide a set of expected results, replacing the ~~or each~~ at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model, resimulating the model with said expanded set and comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

In the Claims

Applicant has submitted a new complete claim set showing amended claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend pending claims 1, 5-8, 10 and 11 as noted below.

1. (Currently Amended) A method of identifying an inaccurate model of a hardware circuit comprising the steps of:

~~simulating~~ running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level ~~to provide a set of expected results~~;

replacing the at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;

~~resimulating~~ re-running the model ~~with~~ by applying said expanded set of signals to the model to obtain a second set of results; and

comparing the ~~two sets~~ first set of expected results with the second set of results and providing an output signal indicating ~~if~~ that the model is inaccurate if the first set of expected results and the second set of results contradict.

2. (Original) A method as claimed in claim 1, wherein the model is an HDL model.

3. (Original) A method as claimed in claim 2, wherein said plurality of signals are selected from a standard logic package data set comprising one or more simple logic levels and one or more abstract data type levels.

4. (Original) A method according to claim 3 further comprising the step of, when said abstract data type is an X selected from the standard logic package, expanding each X into a 0 and a 1.

5. (Currently Amended) A method as claimed in claim 3, wherein the ~~or each~~ at least one abstract data type level ~~signal~~ is converted into two simple logic signals.

6. (Currently Amended) A method according to claim 1, further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with ~~the~~ results from ~~the simulation of~~ running an analog model of the circuit, identifying whether the digital model is an accurate model and only comparing the digital model results with the analog model results if the digital model is determined ~~in said comparing step~~ to be accurate.

7. (Currently Amended) A method according to claim 6, in which said analog model is a SPICE model of the hardware circuit ~~test cell~~.

8. (Currently Amended) A method according to claim 1, further comprising the steps of during running the model ~~simulation for the plurality of signals~~ determining the value of each output from said model; and

during ~~resimulation~~ re-running the model determining for the expanded set of signals the value of each output from the model.

9. (Previously Presented) A method as claimed in claim 1, wherein said model is a digital model.

10. (Currently Amended) A system for identifying an inaccurate model of a hardware circuit comprising:

means for ~~simulating~~ running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level ~~to provide a set of expected results~~;

means for replacing the at least one ~~or each~~ abstract data ~~tpe~~ type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;

means for ~~resimulating~~ re-running the model by applying ~~with~~ said expanded set of signals to the model to obtain a second set of results; and

means for comparing ~~the two sets of~~ the first set of expected results ~~and~~ with the second set of results and providing an output signal indicating ~~if~~ that the model is inaccurate if the first set of expected results and the second set of results contradict.

11. (Currently Amended) A system as claimed in claim [[9]] 10, wherein said system is a computer system.

12. (Previously Presented) A computer program comprising program code that, when executed on a computer, performs any of the steps of any of claims 1 to 9.

inputs. As a result analog simulators provide very accurate descriptions of the designed device operation. However simulation times can be prohibitively protracted especially when a design comprises many thousands or hundreds of thousands of cells to be simulated.

As a solution to the task of describing circuits of such large scale, digital simulators have been developed. Numerous digital simulators have been developed to model the behaviour of circuitry described using a hardware description language (HDL). HDL is a programming language which has been designed and optimised for simulating and thereby describing behaviour of digital circuitry. HDL allows electrical aspects of circuit behaviour to be precisely described. However since only digital signals (which have one of two states) are simulated simulation time scales are much reduced. Additionally, only changes of logic level trigger an evaluation of the effect. A specific example of HDL is the very high speed integrated circuit HDL known as VHDL.

HDL models typically provide a behavioural description of the circuitry of the designed device which can be synthesised into a net list which includes circuit diagrams of the device saved in textual form. In other words, the circuitry of the device is broken down into cells or small circuit portions, each of which has a known behaviour. These cells or small circuit portions are listed in the net list. Operation of the device is simulated by stimulating the net list by the application of a test bench. Test benches are HDL descriptions of circuit stimulus. The outputs of the cell in response to stimulus are compared with expected outputs to verify the behaviour of a circuit over time. The verification results may be analysed to establish how the circuit has functioned.

A problem is that whilst various cells whose operation has an analog type behaviour are modelled as a VHDL behavioural description or a net list of transistors there is no real verification between the cells response in a true analog simulator such as ELDO. As the cells are analogue cells, the

14. /*end of VHDL code

Line 1 is simply a comment which allows the user to make notes referring to the code as a memory aid. The /* and */ notation indicate the start of a comment and the end of the comment respectively. This instructs the compiler to ignore the line of VHDL as the first line does not contain instructions for the compiler.

Lines 2 and 3 are a library clause (library IEEE) and a use clause (use IEEE.STD_LOGIC_1164.all;) respectively. These provide the design entity INV with access to all the names declared in the package STD_LOGIC_1164 stored in the library IEEE and particularly in the data type STD_LOGIC.

The data type of a pin sets out the values of different signal strengths and signals which may flow through the pin.

VHDL supports many such data types which are of an abstract nature including unknowns and high impedance. In order to cater for such abstract values a standard, numbered 1164, has been adopted by the IEEE. This standard defines a standard package containing definitions for a standard 9-valued data type. The standard data type is called standard logic and the IEEE 1164 package is sometimes referred to as the standard logic package or MVL 9 (for multi-value logic 9 values). The standard also defines the logical operations for theses data types, for example the NOT operation.

Each of the nine states of the IEEE 1164 standard logic package are explained below.

'U' : This represents a strong unknown, that is as an input a 'U' indicates anything from a strong low to a strong high. If a 'U' is an output nothing has modified the outputs.

'X' : This also represents a strong unknown and can be anything from a strong low to a strong high signal. In

particular 'X' on an output can indicate that an error has occurred as the signal has passed through the model.

'-' : This also represents a strong unknown and as such can be anything from a strong low to a strong high signal. This is sometimes referred to as NOT 'X'. It can provide a good logic level but it is a don't care state where its actual value is unimportant.

'W' : This state is a weak version of the 'X' data type noted above.

'L' : This data type represents a weak low, that is a low signal having a weak drive strength. This state can also represent a charge storage when used as an output state.

'H' : This is exactly the same as an 'L' however in the opposite sense, that is say it represents a weak high.

'0' : This is a strong low which can be input directly into a model.

'1' : This is a strong high and is the same as a 0 but in the opposite sense.

'Z' : This represents a high impedance signal and when used as an input it means nothing drives the node.

Referring back to the VHDL description of the invention, line 4 provides an arbitrary level to the design entity. This line starts the definition of a new VHDL design unit. Because the library and use clauses are written before the entity declaration they do not begin the VHDL description of the design unit, there are merely context clauses.

The entity declaration includes port declarations which are in lines 5 to 9. Ports may be pins on ICs or any other edge connection on a board etc. Technically ports are signals and so signals and ports are read in the same way. The port

declaration includes the name of each port, the direction in which information is allowed to flow through the ports and the data type of the ports as described above. The entity declaration is completed by the VHDL word ``end''. ``A'' is therefore an input and ``F'' an output.

The architecture body, which is in lines 10 to 13, represents the internal behaviour and structure of the design entity and is itself given an arbitrary name, in this case V1. The VHDL word ``begin'' signifies the start of the architecture statement part. The next line, line 12, is a concurrent signal assignment which describes how the design entity will actually function. This line of code is executed each time the input changes value after a time T which can be defined elsewhere. In the case of an inverter the output F is defined as being equal to NOT the input A. The architecture word ``end'' is used to complete the architecture declaration. The final VHDL comment on line 14 signified by /* is again merely a memory aid.

VHDL can be used to describe more complicated calls.

Figure 2 shows how an ELDO Spice analog simulator might function to model the same inverter. The analog model includes an input A and an output F similar to the VHDL model. However the analog model describes the function of the analog inverter in relation to the transistors 21 and 22 which are arranged in a conventional inverting array. It will be appreciated that analog simulators can model analog voltage sweeps which are not available to the digital level VHDL models. That is the analog simulator can model voltages between the ``0'' and ``1'' levels. A portion of the program code which is executed by the analog model is set out below:

```
1. .subckt INV A F
2. M1 VDD A F PMOS
3. M2 GND A F NMOS
4. .ends
```

As a consequence digital modelling is typically used, especially where the device design being tested includes large quantities of hardware cells. Verification between the cells response in a true analog simulator (ELDO) and its response in the VHDL model is made. Without this verification, a cell which is tested using the quicker VHDL model may be found to be inoperational when using real data types. Embodiments of the present invention overcome the need for the model writer to make such a verification. This is achieved by automating the verification process as far as possible.

Embodiments of the present invention use WIF files. A WIF (waveform interface format) file is an ASCII based file which contains information needed to describe the model's interface (names of ports, directions of signals - input/output/bi-directional, and types of signals) and signal activity against time in a tabular format. In embodiments of the present invention, the IEEE 9 logic states discussed previously are used to indicate both driven and driving states. The pin direction is then used to determine what needs to be done to either drive the value or test for the existence of a value in one of the many supported simulators. Additional parameters can be spec5ified using specially defined comments. These are then used to alter the behaviour of the tool and the simulations/interpretations performed by the tool.

WIF2TB is a program or tool embodying the invention. The program WIF2TB (a flow diagram of which is shown in Figure 6) takes a set of vectors using all nine VHDL logic types and proves by multiple simulations that the VHDL model behaviour is the same as the ELDO simulation. A tool generates an ELDO Spice test bench that reliably reproduces the meanings of the VHDL 9 state logic for use with a Spice model of the circuit under test. The result is a VHDL model which can be added into a VHDL test bench to provide an analog model. This test bench -is connectable to all the ports of the analog model to enable the states of the inputs, outputs and bidirectional pins or the like to be monitored. The tool requires only an input WIF file specifying the pins and vectors. Using this

results for each new vector. Further, any 'Z's on the outputs are expanded into two vectors to allow the program to test for 'Z's in the ELDO simulation.

All this data is then used to write an ELDO test bench that connects to the cell's inputs via a digital to analog converter (DAC) and which can drive the pin to a high or low voltage with different drive strengths. The test bench can also set up a potential divider to provide midband voltages. The actual type of DAC is determined for each pin depending upon what logic states it needs to produce for the simulation. For normal output pins a potential divider is connected to effectively try to force the output pin to a weak unknown. For pins with varying strengths of output another type of DAC is connected that always tries to drive the pin to a midband voltage using a weaker strength drive than should be present on the output. For an output at high impedance a very weak drive is used to drive the pin low then high to try to prove the pin is floating. All the information to do this is held in the program's working memory.

After the simulation has been run the results are converted into an ASCII WIF file. This is then read into the program, where it can be compared to the expected reference results from the VHDL simulation. Only outputs at 0, 1, L, H and Z are checked as all other states are safe unknowns.

The third stage takes place after the ELDO simulation is carried out using the expanded logic package the results are verified against the expected reference results from the VHDL simulation. Not only can the tool check that the outputs match but further verifications can be made to the results to find potential bad transitions.

In summary, embodiments of the present invention provide a tool which is able to generate an ELDO or other suitable SPICE test bench that reliably reproduces the meanings of the VHDL 9 logic states which can then be used in the SPICE model under test. In the tool embodying the invention, the circuit to be

TABLE T.1

The resistors R1 have the lowest resistance and are used to drive strong signals. The resistors R2 are used for the strong edge of the weak drive strength band. The resistors R4 have the highest resistance and are used to produce the very weakest signals.

In the following, R1 can have a resistance of 100Ohms, R2 a resistance 100K Ohms, R3 a resistance of 250 K Ohms and R4 a resistance of 1 MegaOhm. These values are by way of example only.

In Figure 3, resistor (R1) 302 is connected between high voltage supply rail VDD and the input to the analog model. This provides the strong 1 state to the analog model. Analogously resistor (R1) 303 is connected to the ground GND supply rail to supply strong 0 signals as inputs to the analog model. In this way inputs to the analog model which are identified as never changing state can be tied off to one of these inputs depending upon whether they are permanently strong high or low signals. This is provided by the first algorithm.

Resistor (R1) 304 is connected between a control input port 306 and the input to the hardware cell 301. By inputting a series of 0 and 1 signals as control signals on terminal 306 a series of strong 0 and 1 signals can be applied to the cell. This is provided by the second algorithm.

The following are used by the third algorithm. Signal generating circuits 308 and 309 each include a voltage control switch connected to a resistor R2. These resistors have an approximate value of 100kOhms. The circuit 308 is connected to the ground line whilst circuit 309 is connected to the high voltage supply line VDD. Each voltage controlled switch is operable in response to control signals input on control input terminals 310 and 311 respectively. The inputs on these

LEVELS	DIRECTION	RESISTOR USED	SENSE
Strong `0', `1'	Input	1	Not inverted
Strong `0', `1'	Output/Bidirectional	2	Inverted
Z-0, Z-1	Input/Bidirectional	4	Not inverted
Z-0, Z-1	Output	4	Inverted

TABLE T.2

Any signals left to generate are a mix of drive strengths and logic levels. These cases may also have midband voltages. The stimulus for these are made by generating control sequences from pattern generating voltage sources that switch on and off the voltage controlled switches. Each switch connects to the required supply by the required resistor. The pattern generating control supplies are named using numbers to identify the required effect. These are index numbers. When a 1 is output the corresponding voltage and drive strength determined by the resistor used is output. When the control sequence signal is low on a voltage controlled switch the element is tristated from the pin. The following table defines what the index number of each control voltage drives:

INDEX	VOLTAGE	RESISTOR USED
1	V_{DD}	R1
2	V_{DD}	R2
4	V_{DD}	R3
8	V_{DD}	R4
16	GND	R1
32	GND	R2
64	GND	R3
128	GND	R4
256	MID	R1
512	MID	R2
1024	MID	R3

2048	MID	R4

TABLE T.3

As an example consider a 1 pin input which is always driven strongly. In such a case a user would write an ASCII file of the form set out below:

Objects

```
  /name/A:I STD_logic
End
0ns:0
5ns:1
10ns:0
15ns:X
```

The WIF2TB tool would read this into its memory. Firstly the cell name would be read in, then the pins would be defined. In this case there is only one input and that is labelled A.

I is used to indicate an input, O an output, B a directional pin, and S a signal. The signal S is treated as a bidirectional pin.

The type of input is defined as being of the standard logic type. The levels of the signals are defined below as 0 in the first time period at 0ns, followed by 1 in the next time period at 5ns, followed by 0 in the next time period at 10ns followed by an 'X' in the next time period at 15ns. The tool also reads in the timing sequence for the signals on the pin A. These are read in as the time units in this case 5 nanoseconds, a conversion rate 1×10^{-9} and then a series of vectors which are formed by analysing the time details and making the steps between the data signals to be an integer number of small time periods. The tool will then analyse the input levels to identify any complex data states such as 'X's which will require expansion into further 0 and 1 states which can be applied to the analog model. As a result the 010X

simulation of a cell is far more time consuming than running an HDL model a check may first be made on the HDL model by expanding each X on the input.

The first step is to run a first HDL simulation as set out below.

```
Objects
   /AND /A: I STD_Logic
   /AND /B: I STD_Logic
   /AND /F: 0 STD_Logic
End
0ns  : 0 0  0
5ns  : 0 1  0
10ns : 1 0  0
15ns : 1 1  1
20ns : X 0  0
25ns : 0 X  0
30ns : X 1  1
```

This provides the necessary information for the HDL model to read in the data according to that shown in Table T4 having the two inputs A and B and an output F all of which may be selected from the standard logic package. In this step X's is on the inputs are left as an X in the simulation. The output column shown as the third column in Table T4 is then stored as a set of expected results from the HDL model.

As a next step each X on the input is expanded into a 0 and a 1. This results in the input data set out below.

```
0ns  :    0 0
5ns  :    0 1
10ns :    1 0
15ns :    1 1
20ns :    0 0
25ns :    1 0
30ns :    0 0
35ns :    0 1
```

First, reference will be made to Figure 6 which shows a flow diagram of the steps carried out by the tool embodying the present invention.

In step S1, the process starts. In step S2, the first WIF file for the inputs is read and stored in a memory. In step S3, the voltages applied to the bidirectional pins are altered so that 0 is changed to L, 1 to H and X to W. In step S4, the VHDL test bench is written out and the control file for the simulator is also written out. In step S5, the VHDL test bench is analysed. The test bench information is read and converted into a form in which it can be used in the simulation.

In step S6, the VHDL is simulated, the results are converted from a binary representation to an ASCII file and the assertions are checked. Assertions may indicate that certain effects have occurred. These may be error conditions.

In step S7, a second WIF file for the outputs is read into memory. In step S8, the output patterns are copied into the original database. In steps S9, S10 and S11, the Xs are expanded. \`X's are expanded. In step S9, level sensitive \`X's are expanded. In step S10 edge sensitive X's are expanded. In step S11, double edged \`X's are expanded.

In step S12, the second VHDL test bench is written out along with the control file. In step S13, the VHDL test bench is analysed. In step S14, the second VHDL simulation is run, the results are converted and the assertions checked.

In step S15, the output/input Zs are expanded.

In step S16, the ELDO file is written and in step S17, the ELDO test bench is simulated and the results are converted to a WIF file. In step S18, the WIF file is read in to memory (the second database). In step S19, the results are verified and step S20 is the end.

W2TB-I-ASSERT, Adding output testing code

SECTION 11 - the second HDL simulation (steps S13 and S14)

W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16_.vhd'

W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16_behav.vhd'

W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16.netlist'

W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16_cfg.vhd'

W2TB-I-SYSCMD, Running system command 'vhdlan -nc -i w2tb_all_cct_16.control'

SECTION 12 - this checks if the X modelling is correct. If it is, no assertions will be detected. (step S14)

W2TB-I-ASSERT, no assertions detected in last simulation.

W2TB-I-SYSCMD, Running system command 'wif_print ALL_CCT_TEST_BENCH.ow>w2tb'

SECTION 13 Data prepared for SPICE (step S15)

W2TB-I-ZS, Expanded output Z states, now have 204 vectors

SECTION 14 - write SPICE test bench (step S16)

W2TB-I-RES, A total of 6 resistors written to the ELDO test bench

W2TB-I-SW, A total of 72 switches written to ELDO test bench

W2TB-I-VOLT, A total of 76 voltage sources written to ELDO test bench

W2TB-I-CURRENT, a total of 0 current sources written to ELDO test bench

W2TB-S-END, ELDO test bench written

SECTION 15 - run SPICE simulation (step S17)

W2TB-I-SYSCMD, Running system command '$eldodir/com/eldo-stveer w2tb_all_cct

W2TB-I-LOG the log of the eldo simulation has the following lines in it

**** 0 errors

```
**** 0 errors
**** 0 warnings
**** 0 warnings
```

SECTION 16- convert SPICE to WIF file, outputs only (step S17)

```
W2TB-I-SYSCMD, running system command
'$WIF2TB_ROOT/bin/chi2halfwif w2tb_all_
C2W-I-START, Converting ELDO chi file 'w2rb_all_cct_32.chi' into WIF file 'w2
C2W-I-SIGNALS, Found 7 signal to convert
C2W-I-DONE, converted 269 vectors
```

SECTION 17 - read in WIF file, reuse second database in memory (step S18)

```
W2TB-I-WIFIN, Parsing ELDO results wif file
WP-I-PINS, Encountered 7 pins in object block
WP-I-OIN, Read in object block
WP-W-PROGRESS, Percentage of vectors parsed= 100% - completed
WP-I-VECS, Total of 269 vectors read
WP-I-DELTA, Smallest delta = 100.00 ps
WP-I-PIN, Read in the test patterns
W2TN-S-IN, Successfully loaded ELDO database
```

SECTION 18 - check all pins (step S19)

```
W2TB-I-VERIFY, Verifying pin 'f1'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f2'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f3'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f4'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f5'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f6'
W2TB-I-STAT, This pin passed all the tests
W2TB-I-VERIFY, Verifying pin 'f7'
W2TB-I-STAT, This pin failed 1 times
WT2B-I-STAT, A total of 1 pins failed verification
```

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

or Fax **(703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 04/15/2005

James H Morris
Wolf Greenfield & Sacks PC
600 Atlantic Avenue
Boston, MA 02210

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

Gail Driscoll	(Depositor's name)
Gail Driscoll	(Signature)
7-15-05	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,422	10/19/2000	Peter Ballam	S1022/8545	6731

TITLE OF INVENTION: METHOD OF IDENTIFYING AN ACCURATE MODEL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$0	$1400	07/15/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
PALADINI, ALBERT WILLIAM	2125	703-014000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Lisa K. Jorgenson
2 James H. Morris
3 Wolf, Greenfield & Sacks, P.C.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
STMicroelectronics Limited

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Almondsbury Bristol, United Kingdom

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies 10

4b. Payment of Fee(s):
- ☒ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 23/2825 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature ______ Date 6/20/05

Typed or printed name James H. Morris Registration No. 34,681

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.